

1 1. A method comprising:
2 machining a hole on an integrated circuit with a
3 scanning probe system; and
4 performing a circuit edit through the hole formed
5 by said system.

1 2. The method of claim 1 including machining said
2 hole on the backside of the integrated circuit.

1 3. The method of claim 2 including machining a hole
2 as a series of progressively smaller trenches through the
3 backside of a silicon wafer.

1 4. The method of claim 1 including providing an
2 electrical connection between said integrated circuit and
3 said tool.

1 5. The method of claim 3 including detecting an open
2 circuit when the tool reaches an isolation region.

1 6. The method of claim 3 including detecting a short
2 circuit when the tool reaches a metallization.

1 7. The method of claim 1 including covering a
2 portion of said hole with an insulating layer.

1 8. The method of claim 7 including covering said
2 hole with an insulating layer before exposing a
3 metallization.

1 9. The method of claim 1 including spring biasing a
2 cantilever of an atomic force microscopy tool against an
3 integrated circuit.

1 10. A method comprising:
2 forming a first trench having sidewalls and a
3 bottom in a semiconductor structure using a scanning probe
4 system;
5 forming a second trench through said bottom, said
6 second trench having sidewalls that are spaced more closely
7 than the sidewalls of said first trench; and
8 using said trench to perform a circuit edit.

1 11. The method of claim 10 including biasing an
2 atomic force microscopy tip against the semiconductor
3 surface to move atomic layers to form said trenches.

1 12. The method of claim 11 providing an electrical
2 connection between said semiconductor structure and said
3 tip.

1 13. The method of claim 12 including detecting an
2 open circuit when said tip reaches an isolation region in
3 said semiconductor structure.

1 14. The method of claim 12 including detecting a
2 short circuit once the tip reaches a metallization in said
3 semiconductor structure.

1 15. The method of claim 10 including covering said
2 first and second trenches with an insulating layer.

1 16. The method of claim 15 including covering said
2 trenches with an insulating layer before exposing a
3 metallization.

1 17. The method of claim 11 including spring biasing
2 said tip against said structure using a cantilever.

1 18. The method of claim 17 including determining the
2 position of said tip by reflecting a laser beam from said
3 cantilever.

1 19. An atomic force microscopy tool comprising:
2 a cantilever to penetrate an integrated circuit;
3 a tip coupled to said cantilever; and

4 a circuit including a voltage source coupled
5 between said tip and an integrated circuit.

1 20. The tool of claim 19 wherein said circuit
2 includes an ammeter.

1 21. The tool of claim 19 wherein said circuit is
2 connected to a metallization in said integrated circuit
3 such that once the tip contacts said metallization, a short
4 circuit is created.

1 22. The tool of claim 19 wherein an open circuit
2 exists when said tool tip is electrically isolated from
3 said metallization.